Titles of most frequently occurring classifications of patents returned from a search of 10826954 on Dec 18 , 2006

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 14  324/754       (8 OR, 6 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/500       .FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC
COMPONENTS
          324/537       ..Of individual circuit component or element
          324/754       ...With probe elements

  5  324/72.5      (0 OR, 5 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/72        .TESTING POTENTIAL IN SPECIFIC ENVIRONMENT (E.G., LIGHTNING
STROKE)
          324/72.5      ..Voltage probe

  5  324/758       (4 OR, 1 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/500       .FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC
COMPONENTS
          324/537       ..Of individual circuit component or element
          324/754       ...With probe elements
          324/758       ....Probe alignment or positioning

  4  324/761       (4 OR, 0 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/500       .FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC
COMPONENTS
          324/537       ..Of individual circuit component or element
          324/754       ...With probe elements
          324/761       ....Pin

  4  324/757       (1 OR, 3 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/500       .FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC
COMPONENTS
          324/537       ..Of individual circuit component or element
          324/754       ...With probe elements
          324/757       ....Probe contact enhancement

  4  439/66        (4 OR, 0 XR)
          Class 439     ELECTRICAL CONNECTORS
          439/55        .PREFORMED PANEL CIRCUIT ARRANGEMENT, E.G., PCB, ICM, DIP,
CHIP, WAFER, ETC.
          439/65        ..With provision to conduct electricity from panel circuit
to another panel circuit
          439/66        ...Conductor is compressible and to be sandwiched between
panel circuits

  3  977/875       (0 OR, 3 XR)
          Class 977     NANOTECHNOLOGY
          977/840       .MANUFACTURE, TREATMENT, OR DETECTION OF NANOSTRUCTURE
          977/849       ..With scanning probe
          977/860       ...Scanning probe structure
          977/875       ....With tip detail

  3  324/762       (2 OR, 1 XR)
          Class 324     ELECTRICITY:  MEASURING AND TESTING
          324/500       .FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC
COMPONENTS
          324/537       ..Of individual circuit component or element
          324/754       ...With probe elements
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          324/762       ....Cantilever

  3  204/403.01    (1 OR, 2 XR)
          Class 204     CHEMISTRY:  ELECTRICAL AND WAVE ENERGY
          204/193       .APPARATUS
          204/194       ..Electrolytic
          204/400       ...Analysis and testing
          204/403.01    ....Biological material (e.g., microbe, enzyme, antigen,
etc.) analyzed, tested, or included in apparatus

  3  257/E23.021   (0 OR, 3 XR)
          Class 257     ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE
DIODES)
          257/E23.001   .PACKAGING, INTERCONNECTS, AND MARKINGS FOR SEMICONDUCTOR OR
OTHER SOLID-STATE DEVICES (EPO)
          257/E23.01    ..Arrangements for conducting electric current to or from
solid-state body in operation, e.g., leads, terminal arrangements (EPO)
          257/E23.012   ...Consisting of lead-in layers inseparably applied to
semiconductor body (EPO)
          257/E23.019   ....Consisting of layered constructions comprising
conductive layers and insulating layers, e.g., planar contacts (EPO)
          257/E23.021   .....Bump or ball contacts (EPO)

  3  257/E23.078   (0 OR, 3 XR)
          Class 257     ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE
DIODES)
          257/E23.001   .PACKAGING, INTERCONNECTS, AND MARKINGS FOR SEMICONDUCTOR OR
OTHER SOLID-STATE DEVICES (EPO)
          257/E23.01    ..Arrangements for conducting electric current to or from
solid-state body in operation, e.g., leads, terminal arrangements (EPO)
          257/E23.078   ...Flexible arrangements, e.g., pressure contacts without
soldering (EPO)

  2  257/751       (2 OR, 0 XR)
          Class 257     ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE
DIODES)
          257/734       .COMBINED WITH ELECTRICAL CONTACT OR LEAD
          257/741       ..Of specified material other than unalloyed aluminum
          257/750       ...Layered
          257/751       ....At least one layer forms a diffusion barrier

  2  257/E23.02    (0 OR, 2 XR)
          Class 257     ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE
DIODES)
          257/E23.001   .PACKAGING, INTERCONNECTS, AND MARKINGS FOR SEMICONDUCTOR OR
OTHER SOLID-STATE DEVICES (EPO)
          257/E23.01    ..Arrangements for conducting electric current to or from
solid-state body in operation, e.g., leads, terminal arrangements (EPO)
          257/E23.012   ...Consisting of lead-in layers inseparably applied to
semiconductor body (EPO)
          257/E23.019   ....Consisting of layered constructions comprising
conductive layers and insulating layers, e.g., planar contacts (EPO)
          257/E23.02    .....Bonding areas, e.g., pads (EPO)

  2  439/791       (0 OR, 2 XR)
          Class 439     ELECTRICAL CONNECTORS
          439/775       .METALLIC CONNECTOR OR CONTACT HAVING MOVABLE OR RESILIENT
SECURING PART
          439/790       ..Single operator for securing and joining plural conductors
          439/791       ...Single screw-threaded operator

  2  136/228       (1 OR, 1 XR)
          Class 136     BATTERIES:  THERMOELECTRIC AND PHOTOELECTRIC
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136/200 .THERMOELECTRIC
136/228 ..One junction element surrounded by another junction element

2 257/E21.531 (0 OR, 2 XR)
Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)
257/E21.001 .PROCESSES OR APPARATUS ADAPTED FOR MANUFACTURE OR TREATMENT OF SEMICONDUCTOR OR SOLID-STATE DEVICES OR OF PARTS THEREOF (EPO)
257/E21.521 ..Testing or measuring during manufacture or treatment or reliability measurement, i.e., testing of parts followed by no processing which modifies parts as such (EPO)
257/E21.529 ...Measuring as part of manufacturing process (EPO)
257/E21.531 ....For electrical parameters, e.g., resistance, deep-levels, CV, diffusions by electrical means (EPO)

2 72/458 (2 OR, 0 XR)
Class 72 METAL DEFORMING
72/457 .BY OR WITH WORK-CONSTRAINER AND/OR MANIPULATED WORK-FORCER
72/458 ..Comprising lever manipulated to force work

2 72/479 (0 OR, 2 XR)
Class 72 METAL DEFORMING
72/462 .TOOL AND/OR TOOL HOLDER
72/476 ..Having unitary tool-face
72/479 ...With elongated extension fixed to tool face in use (e.g., handle or shank)

10826954_CLS.txt

Most frequently occurring classifications of patents returned from a search of 10826954 on Dec 18 , 2006

Original Classifications

8	324/754
4	324/761
4	439/66
4	324/758
2	257/751
2	324/762
2	72/458

Cross-Reference Classifications

6	324/754
5	324/72.5
3	324/757
3	977/875
3	257/E23.021
3	257/E23.078
2	257/E23.02
2	439/791
2	204/403.01
2	257/E21.531
2	72/479

Combined Classifications

14	324/754
5	324/72.5
5	324/758
4	324/761
4	324/757
4	439/66
3	977/875
3	324/762
3	204/403.01
3	257/E23.021
3	257/E23.078
2	257/751
2	257/E23.02
2	439/791
2	136/228
2	257/E21.531
2	72/458
2	72/479

EAST Browser - L6: (5) 3 and titanium | US 6339257 | Tag: S,P,T1 | Doc: 5/5 | "Full" 2/11 (Total images 11) | Drawings

U.S. Patent Jan. 15, 2002 Sheet 1 of 6 US 6,339,257 B1

FIG. 1

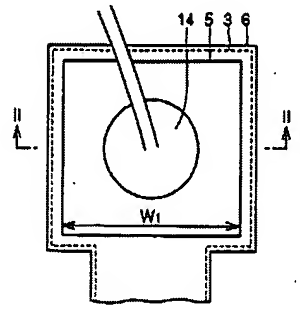

FIG. 2

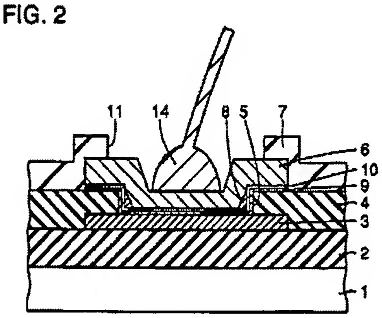

FIG. 2 is a view showing a cross section taken along the line II--II in FIG. 1.

FIGS. 3 to 7 are cross sectional views showing first to fifth steps of a method of manufacturing the semiconductor device shown in FIGS. 1 and 2.

FIG. 8 is a cross sectional view showing a structure of a conventional bonding pad electrode.

FIG. 9 is a cross sectional view showing a bonding pad electrode shown in conjunction with a problem associated with the conventional bonding pad electrode.

FIG. 10 is a cross sectional view showing the bonding pad electrode shown in conjunction with a problem associated with connection of a bonding wire to the bonding pad electrode shown in FIG. 9.

FIGS. 11 to 13 are cross sectional views showing a conventional semiconductor device described in the aforementioned Laying-Open Application.

DETAILED DESCRIPTION:

(1) DESCRIPTION OF THE PREFERRED EMBODIMENTS

(2) An embodiment of the present invention will now be described with reference to the drawings.

(3) Referring to FIGS. 1 and 2, an interlayer insulating film 2 including a silicon oxide film is formed on a silicon substrate 1. An interconnection layer 3 including aluminum is formed on interlayer insulating film 2. An interlayer insulating film 4 as a first insulating layer including a silicon oxide film is formed to cover interconnection layer 3. A via hole 5 is formed in interlayer insulating film 4 as a first hole leading to interconnection layer 3. A length of a side of the via hole (a length corresponding to W.sub.1 in FIG. 1) is about 100 .mu.m. A depth of the via hole is about 1 .mu.m. Via hole 5 allows a surface of interconnection layer 3 to be exposed. A titanium (Ti) layer 9 as a first intermediate layer and a titanium nitride (TiN) layer 10 as a second intermediate layer are formed on the exposed surface of interconnection layer 3, a sidewall of via hole 5 and a surface of interlayer insulating film 4. Titanium layer 9 and titanium nitride layer 10 form the intermediate layer. Titanium layer 9 is in contact with interconnection layer 3 and titanium nitride layer 10. A sidewall conductive layer 8 as a sidewall conductive layer including tungsten is formed in contact with

Details | Text | Image | HTML | FULL

EAST Advanced Find

Find what: nitride

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Area: All / Sel/Cur — Direction: Up / Down — Match word: Whole / Left / Part / Right — Look in: Grid / Documents / Pagemark Comments

Details | Text | Image | HTML | Full

* Consulted SARKAR 4 BVAN

US 20020011669A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2002/0011669 A1

FUJIKI et al. (43) Pub. Date: Jan. 31, 2002

(54) SEMICONDUCTOR DEVICE

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(*) Notice: This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) Appl. No.: 09/352,336

(22) Filed: Jul. 13, 1999

(30) Foreign Application Priority Data

Jan. 28, 1999 (JP) ..... 11-019841 (P)

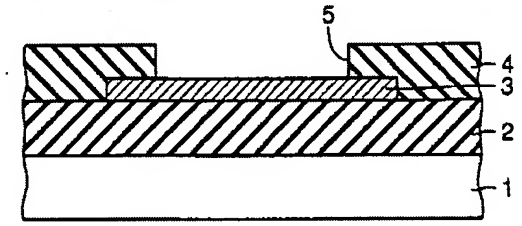
Publication Classification

(51) Int. Cl.[7] H01L 23/48; H01L 23/52; H01L 29/40

(52) U.S. Cl. 257/781

(57) ABSTRACT

A semiconductor device which is provided with enhanced reliability and capable of preventing cracking of a layer below an interconnection layer and separation of the interconnection layer and a bonding pad electrode layer. The semiconductor device includes: an interconnection layer including a conductive material formed on a silicon substrate; an intermediate layer formed in contact with interconnection layer and including a titanium layer and a titanium nitride layer; and a bonding pad electrode layer which is in contact with the intermediate layer.



DOCUMENT-IDENTIFIER: US 20020011669 A1
TITLE: SEMICONDUCTOR DEVICE

Abstract Paragraph - ABTX (1):

A semiconductor device which is provided with enhanced reliability and capable of preventing cracking of a layer below an interconnection layer and separation of the interconnection layer and a bonding pad electrode layer. The semiconductor device includes: an interconnection layer including a conductive material formed on a silicon substrate; an intermediate layer formed in contact with interconnection layer and including a titanium layer and a titanium nitride layer; and a bonding pad electrode layer which is in contact with the intermediate layer.

Pre-Grant Publication (PGPub) Document Number - PGNR (1):

20020011669

Current US Classification, US Primary Class/Subclass - CCPR (1):

257/751

Current US Classification, US Secondary Class/Subclass - CCSR (1):

257/E23.02

Summary of Invention Paragraph - BSTX (20):

[0018] A semiconductor device according to one aspect of the present invention includes an interconnection layer, an intermediate layer and a bonding pad electrode layer. The interconnection layer is formed on a semiconductor substrate. The intermediate layer is formed in contact with the interconnection layer and includes at least one material selected from a group of titanium, molybdenum, tungsten, titanium silicide, molybdenum silicide, tungsten silicide, titanium nitride, molybdenum nitride and tungsten nitride. The bonding pad electrode layer is in contact with the intermediate layer.

Summary of Invention Paragraph - BSTX (21):

[0019] In the semiconductor device having the above described structure, a strength of the intermediate layer is high as it includes at